WHAT IS CLAIMED IS:

1. An information processing apparatus comprising:

semiconductor memory means including a plurality of nonvolatile memory cells;

switch means for turning on and off power supplied for refresh operation of said semiconductor memory means during a nonuse period of the apparatus; and

refresh control means supplied with power at all times even during said nonuse period, for effecting control to turn on said switch means and performing the refresh operation of said nonvolatile memory cells during said nonuse period.

2. The information processing apparatus as claimed in claim 1,

wherein said refresh control means periodically effects control to turn on said switch means;

specifies an address of said nonvolatile memory cell, and performs the refresh operation of said nonvolatile memory cell corresponding to the specified address; and

then effects control to turn off said switch means.

3. The information processing apparatus as claimed in claim 1,

wherein said nonvolatile memory cells have one of:

a structure using ferroelectric film as storing material, and storing data of two values or more by difference in polarization direction of said ferroelectric film;

a structure using magnetic film as storing material, and storing data of two values or more by difference in magnetization direction of said magnetic film; and

a structure using chalcogenide film as storing material, and storing data of two values or more by difference in crystal state of said chalcogenide film.

4. The information processing apparatus as claimed in claim 1,

wherein said switch means and said refresh control means are included within a memory chip including said semiconductor memory means.

5. A semiconductor memory comprising:

a nonvolatile memory cell; and

a signal generating unit for generating a signal to perform refresh operation of said nonvolatile memory cell corresponding to an address inputted to an address terminal in response to turning on of power to a power supply terminal.

6. The semiconductor memory as claimed in claim 5,

wherein said nonvolatile memory cell includes a

ferroelectric capacitor using ferroelectric film as storing material, and storing data of two values or more by difference in polarization direction of said ferroelectric film; and

at a time of said refresh operation, after operation of reading data from a memory cell group to be refreshed, data of "1" is written to said entire memory cell group, and then the data stored in said memory cell group is restored.

7. The semiconductor memory as claimed in claim 5,

wherein said nonvolatile memory cells have one of:

a structure using ferroelectric film as storing material, and storing data of two values or more by difference in polarization direction of said ferroelectric film;

a structure using magnetic film as storing material, and storing data of two values or more by difference in magnetization direction of said magnetic film; and

a structure using chalcogenide film as storing material, and storing data of two values or more by difference in crystal state of said chalcogenide film.

8. A semiconductor memory comprising:

a nonvolatile memory cell;

switch means for turning on and off power supplied

for refresh operation of said nonvolatile memory cell; and

refresh control means supplied with power even during an off period of said switch means, for effecting control to turn on said switch means and performing the refresh operation of said nonvolatile memory cell during said off period.

9. The semiconductor memory as claimed in claim 8,

wherein said refresh control means periodically effects control to turn on said switch means;

specifies an address of said nonvolatile memory cell, and performs the refresh operation of said nonvolatile memory cell corresponding to the specified address; and

then effects control to turn off said switch means.

10. The semiconductor memory as claimed in claim 8, further comprising:

a first power supply terminal supplied with main power;

a second power supply terminal supplied with backup power at all times; and

power sensing means for monitoring a state of power supply from said first power supply terminal, and supplying said refresh control means with a performance

control signal in response to a power supply voltage from said first power supply terminal becoming a predetermined value or lower;

wherein said switch means turns on and off power supplied via said second power supply terminal for the refresh operation of said nonvolatile memory cell; and

said refresh control means effects control to turn on said switch means in response to said performance control signal supplied from said power sensing means and performs the refresh operation of said nonvolatile memory cell.

11. The semiconductor memory as claimed in claim 8,

wherein said nonvolatile memory cell has one of:

a structure using ferroelectric film as storing material, and storing data of two values or more by difference in polarization direction of said ferroelectric film;

a structure using magnetic film as storing material, and storing data of two values or more by difference in magnetization direction of said magnetic film; and

a structure using chalcogenide film as storing material, and storing data of two values or more by difference in crystal state of said chalcogenide film.

12. The semiconductor memory as claimed in claim 8,

wherein said nonvolatile memory cell includes a ferroelectric capacitor using ferroelectric film as storing material, and storing data of two values or more by difference in polarization direction of said ferroelectric film; and

at a time of said refresh operation, after operation of reading data from a memory cell group to be refreshed, data of "1" is written to said entire memory cell group, and then the data stored in said memory cell group is restored.